DESIGN AUTOMATION CONFERENCE 56
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Practical cell based analog design methodology II (AnaCell)

Promotion of analog automatic cell generation with the designability in AnaCell

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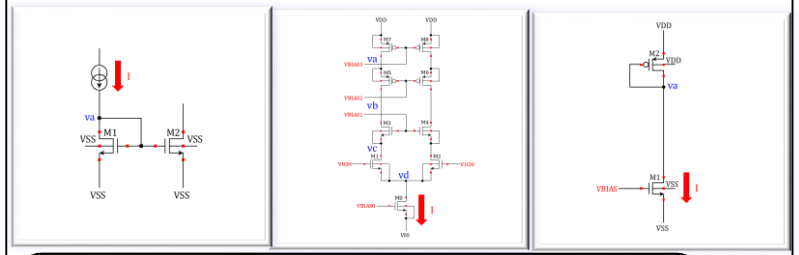
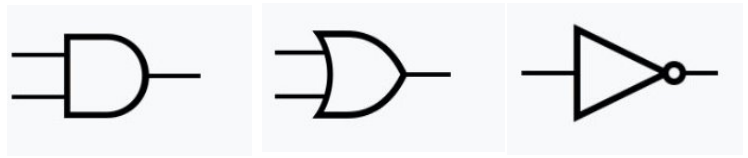
Difficulty of analog standard cell design

Analog Cell



- Cells are highly correlated each other
- Specifications are diverse and continuous
- Number of Cell kinds is unlimited in terms of performance
- Process margin depends on W/L and layout

Digital Cell

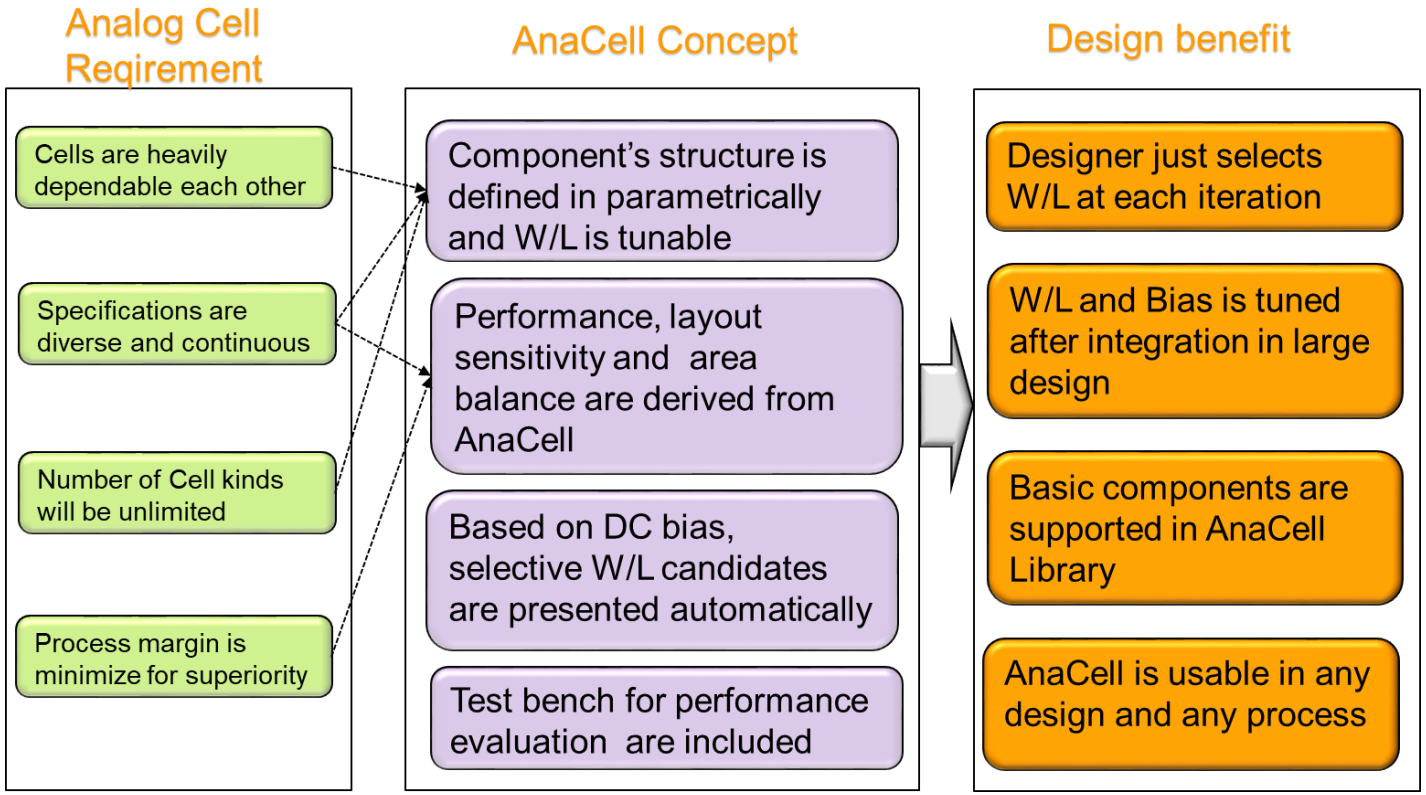


- Cell components are electrically isolated each other
- Specification is limited and discrete
- Number of Cell kinds are limited around hundreds
- Process margin is sufficiently included in cell library

Standard Cell design in Analog could not have been applied like digital design.

Concept of AnaCell and the difficulty

AnaCell is targeting to become like the digital standard cell in Analog Design



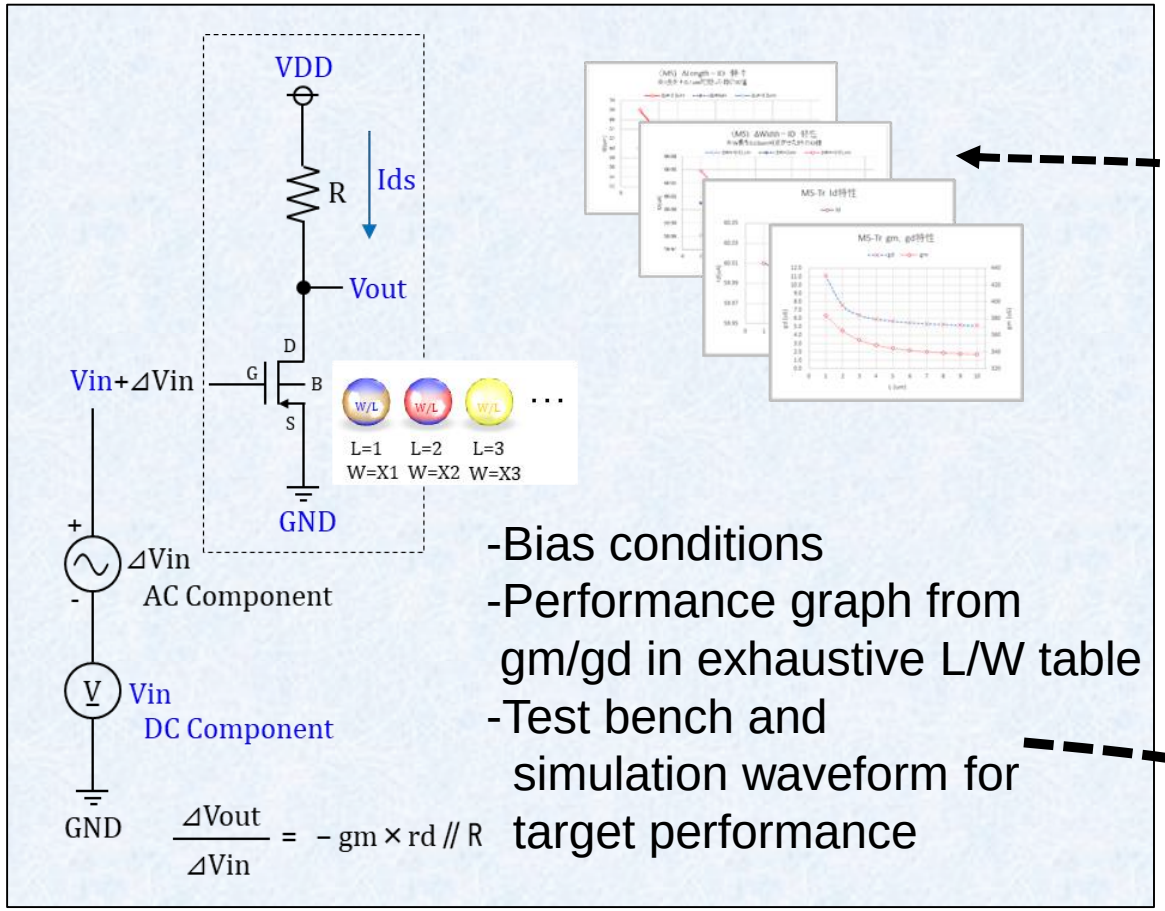
Cell	Type	TR #	Total #
Differential Input	Current mirror	5	24
	Constant current mirror	5	
	Cascode current mirror	7	
	…	7-9	
Current Source	…	2-7	36
Amplification	…	2-4	22

Still designer needs the iteration to find the appropriate DC bias to satisfy the various requirements in AnaCell

-DC bias means circuit's operating points and each Transistors' Vgs/Vds/Vbs etc.

Design methodology using AnaCell

AnaCell



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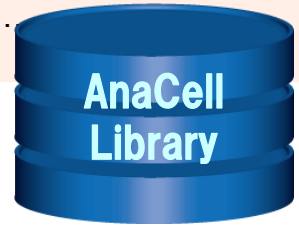
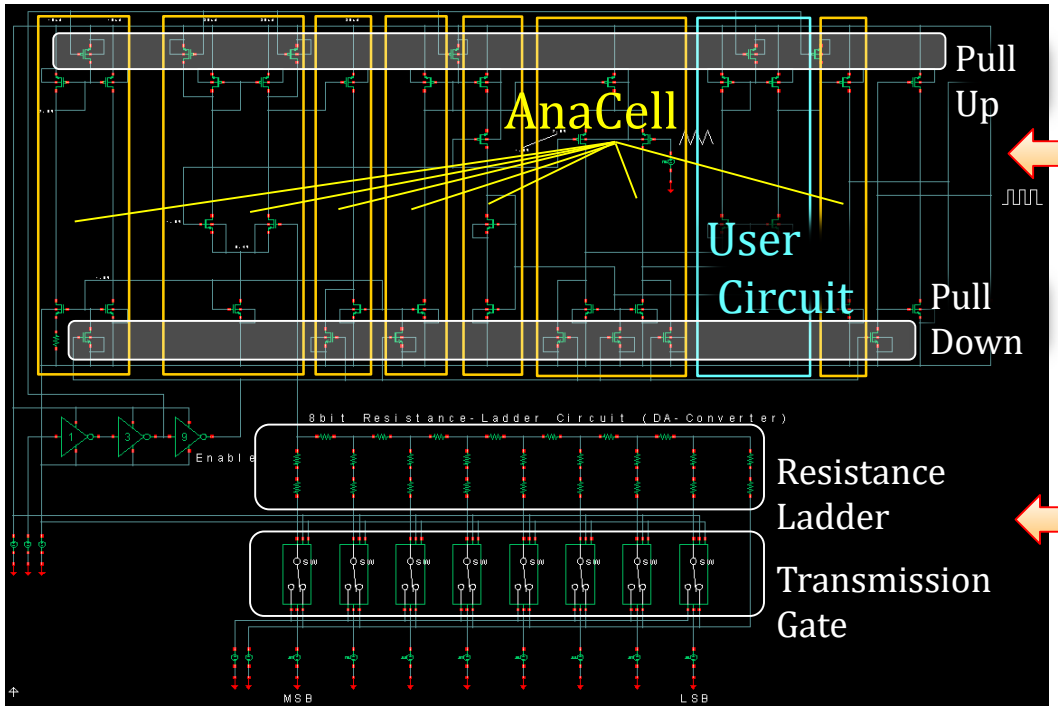


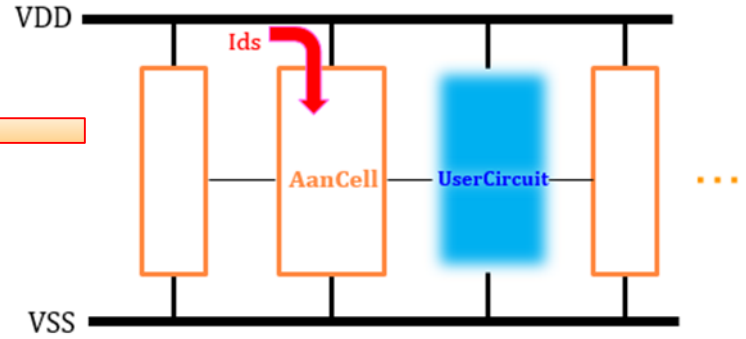
∗ AnaCell is under Patent pending

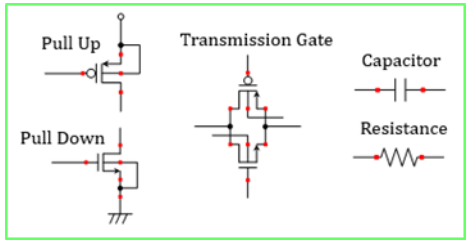
Tuning each transistor's Bias and W/L in AnaCell

AnaCell deign usage

- The circuits that consist of AnaCells are suitable for Current source/OPAMP/Regulator etc.
- There is no limit in circuit size and number of AnaCells for designing
- Circuits can be designed combining AnaCells and Pull UP/Down and Gate elements





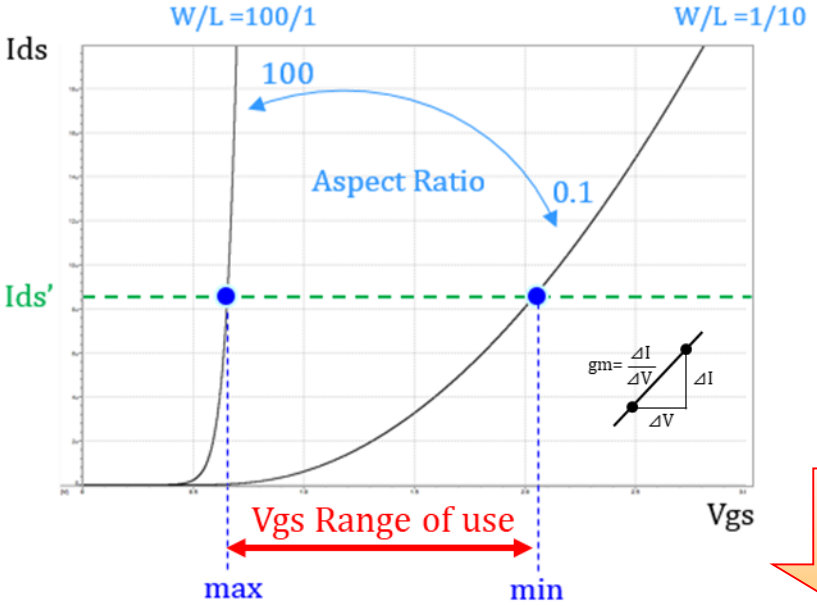


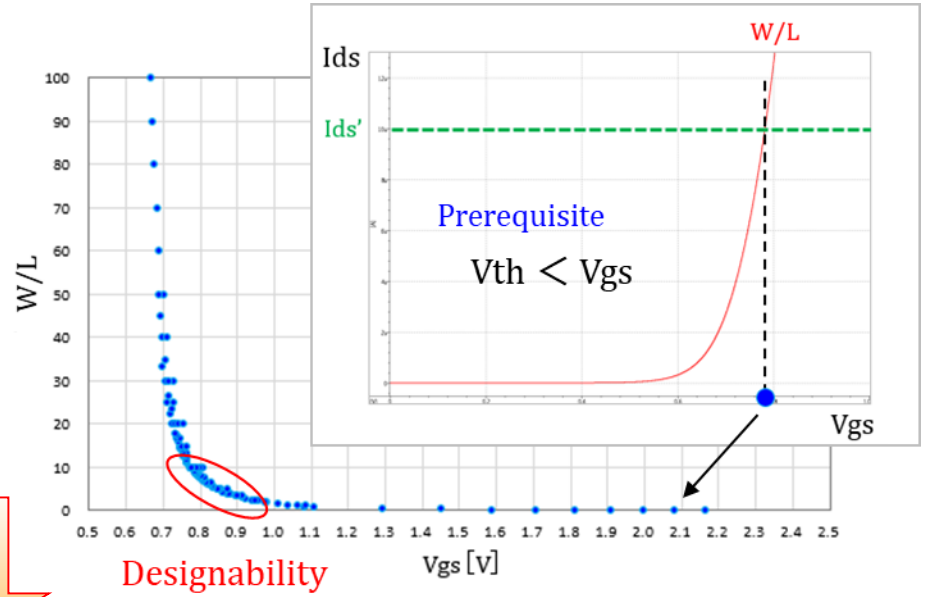
Pulse Width Modulation Circuit

consists of AnaCell/Pullup/RESISTENCE Ladder/Transmission Gate/User Circuit

Concern in DC bias setting and auto selection

- Vgs, Vds has feasible range to derive a certain Ids regarding gm (W/L)
- Design space of W and L is discrete and has specific curve
- Every W/L which satisfies the target Ids may be logically the candidate but in terms of designability for other metrics every W/L does not fully satisfy
- Designability: We define the designability as the freedom and allowance for design L/W for adjusting the multi objects of circuit performance.



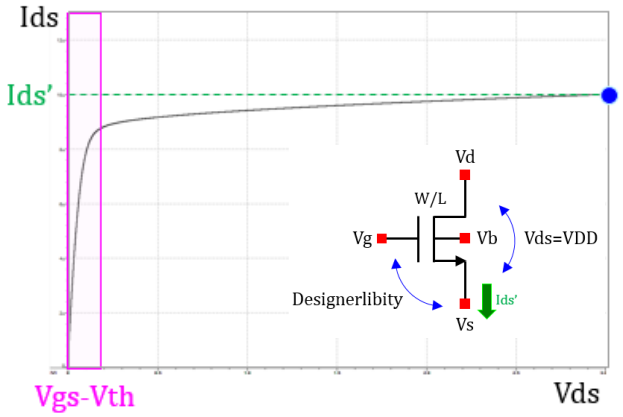


Automatic selection of the DC bias which maximizes the designability should be the best candidates for AnaCell in specific process

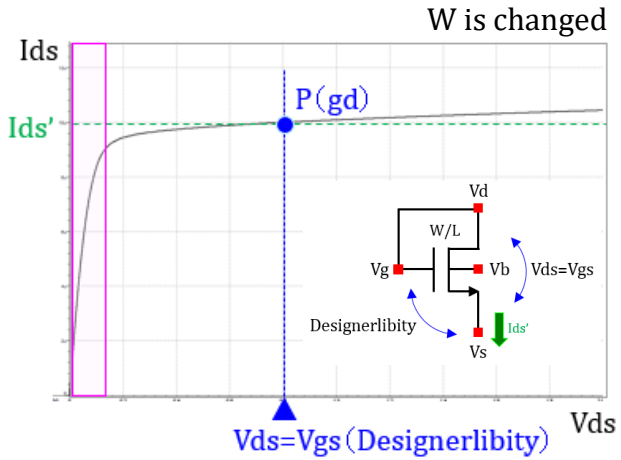
∗ AnaCell is under Patent pending

DC bias setting and Vds tuning 1

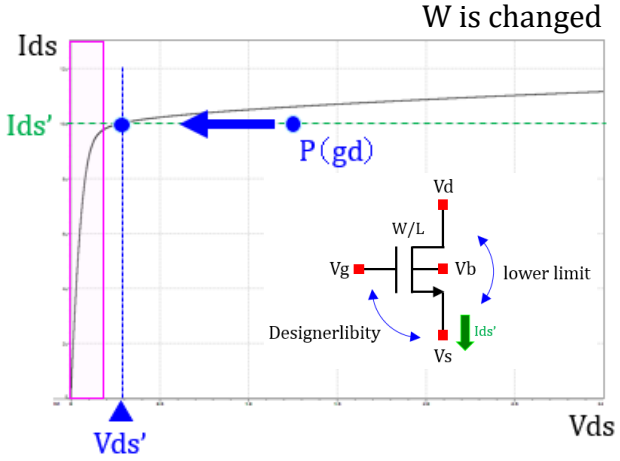
- Each transistor starts from Vds=Vdd
- Valuable Vds of each transistor should be lower than Vdd under the condition of saturation and reasonable gd slope



Point that acquired Vgs (Designability)
Vds>Vgs-Vth ∴Saturation Region



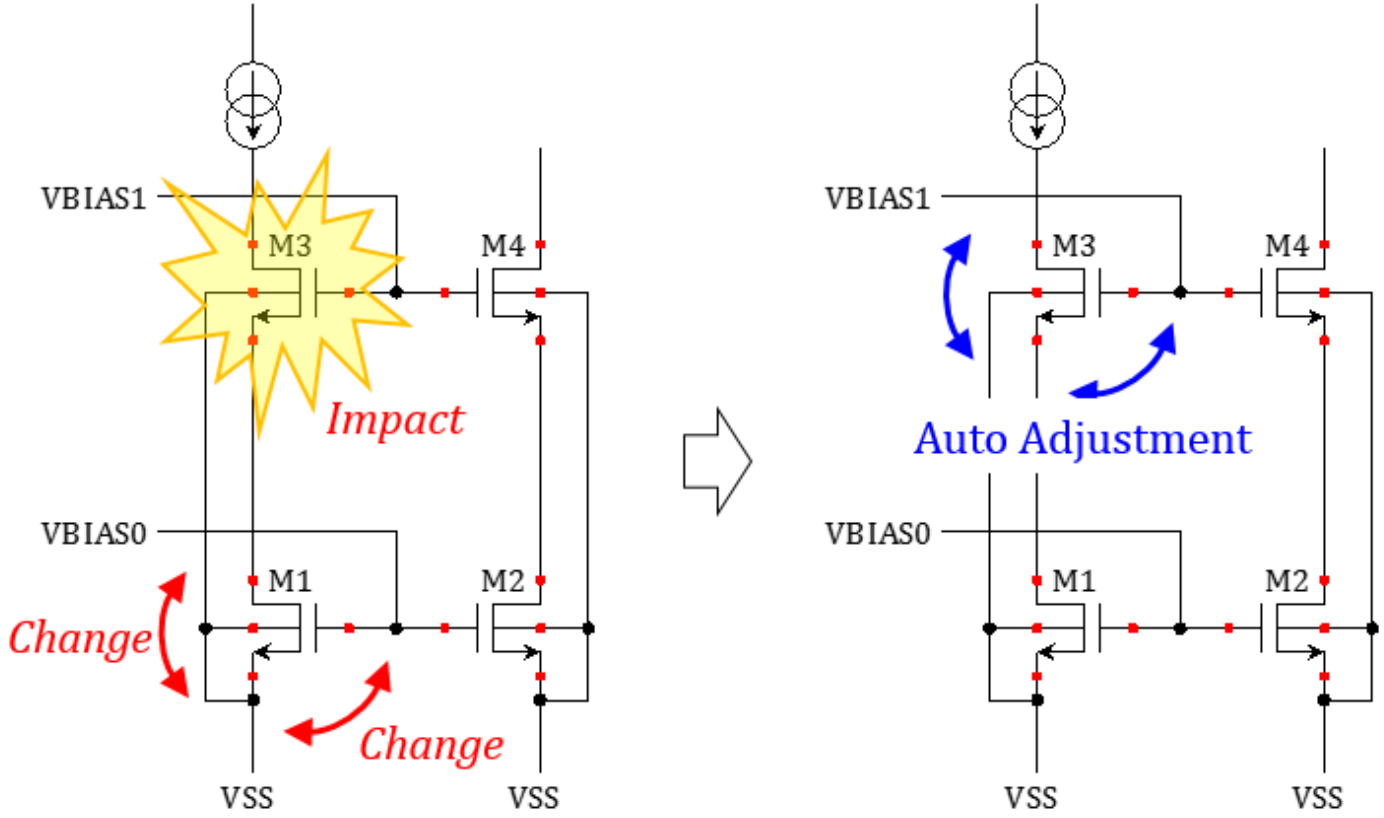
Reference Point of gd (slope) $P(gd)=\frac{\Delta I}{\Delta V}$
Vds=Vgs ∴Saturation Region



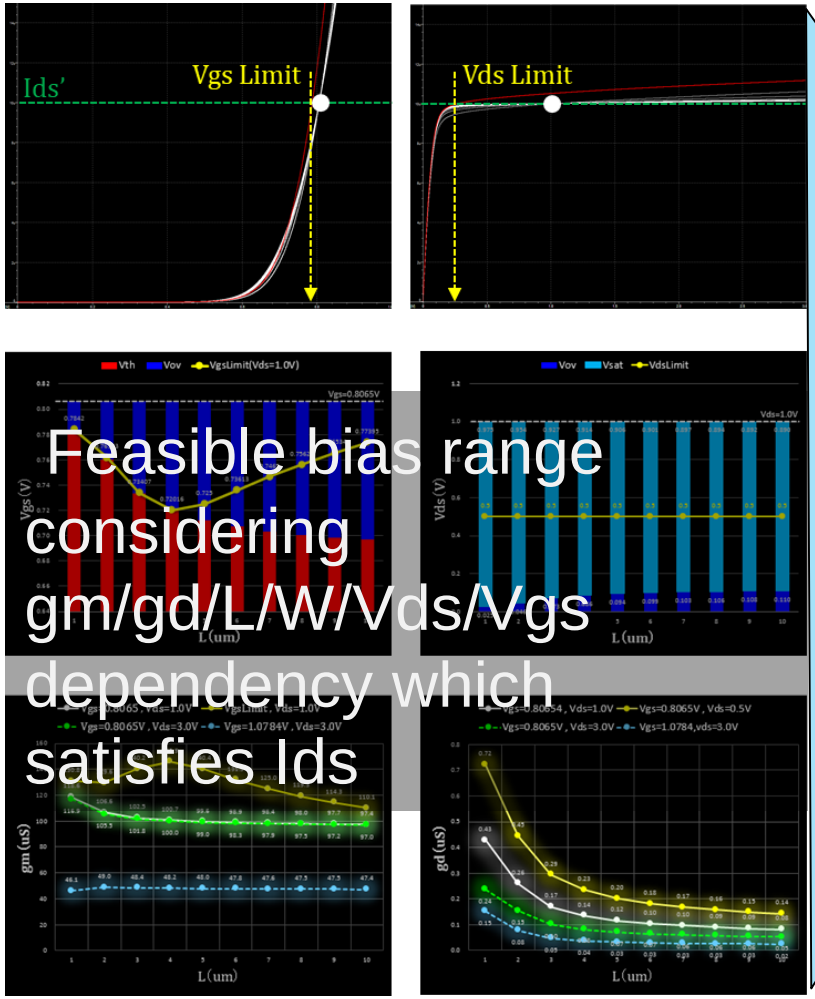
Derive the lower limit Vds' based on gd
Vds>Vgs-Vth ∴Saturation Region

DC bias setting and Vds tuning 2

■Bias of each transistor is automatically adjusted satisfying VDD-GND voltage
■This feature is also interactively usable and fast in manually adjustment without the effort of changing all transistors in AnaCell



Design methodology using AnaCell with auto DC bias setting



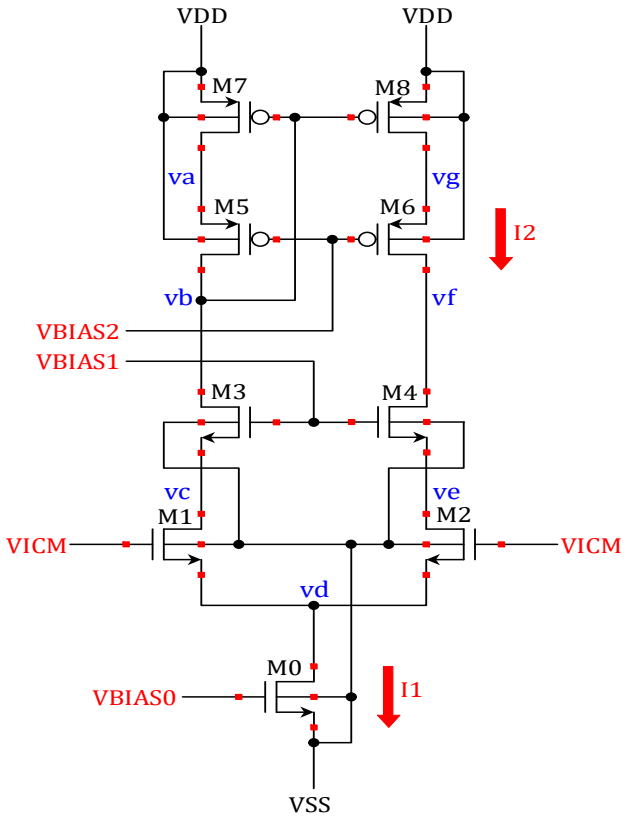
Feasible bias range considering gm/gd/L/W/Vds/Vgs dependency which satisfies Ids

1. Construct Circuit by AnaCell
2. Apply Technology to AnaCell
3. Specify only supply voltage(VDD) and Ids to each AnaCell and get the initial DC bias for all Transistors automatically
4. Select and adjust L W which satisfies AnaCell requirements from candidates
5. Simulation with AC/Transient and evaluate final goal

Designer can instantly get the initial appropriate DC bias under only VDD and Ids current.

2 Experiments in TPSco 65nm PDK

1. Differential Input Circuit Single-Ended Signaling Type Telescopic Current Mirror



Input Value

VDD	3.3
VSS	0
I1	20u
I2	10u

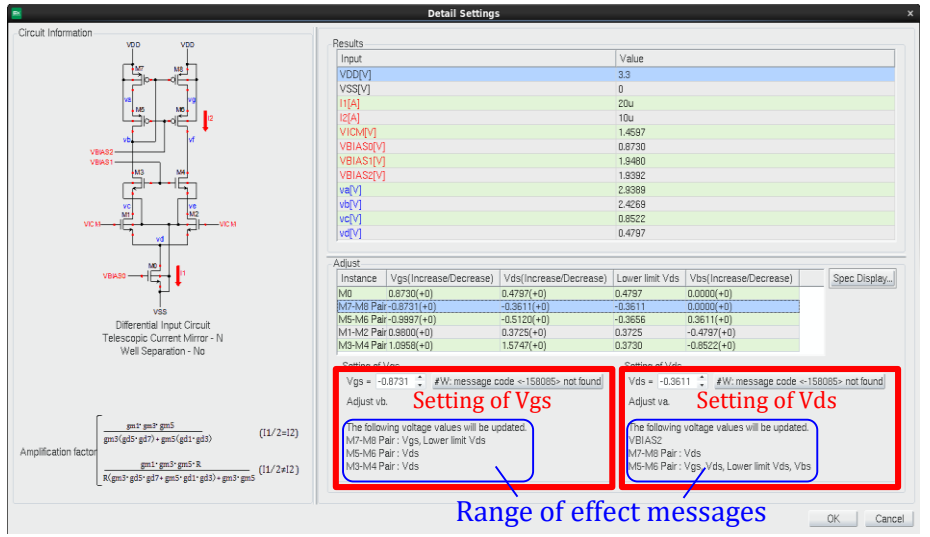
Initial Solution

VICM	1.4598
VBIAS0	0.8730
VBIAS1	1.9462
VBIAS2	1.8441
va	2.9060
vb	2.3778
vc	0.8508
vd	0.4798

Result

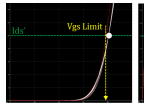
W/L Combination	81000
Gain	79.5 ～ 110.2dB

Initial Value

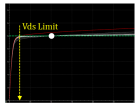


Bias Adjustment

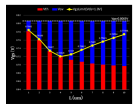
Ids-Vgs



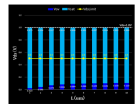
Ids-Vds



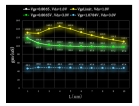
Vgs-Limit



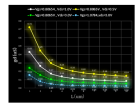
Lower Limit Vds



gm parameter at DC Bias Point



gd parameter at DC Bias Point

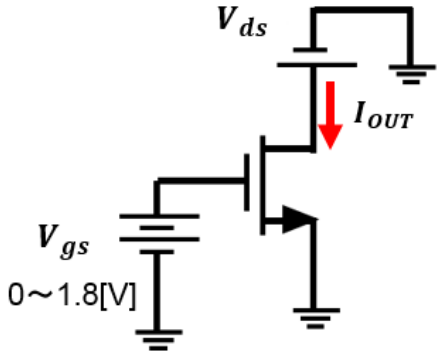


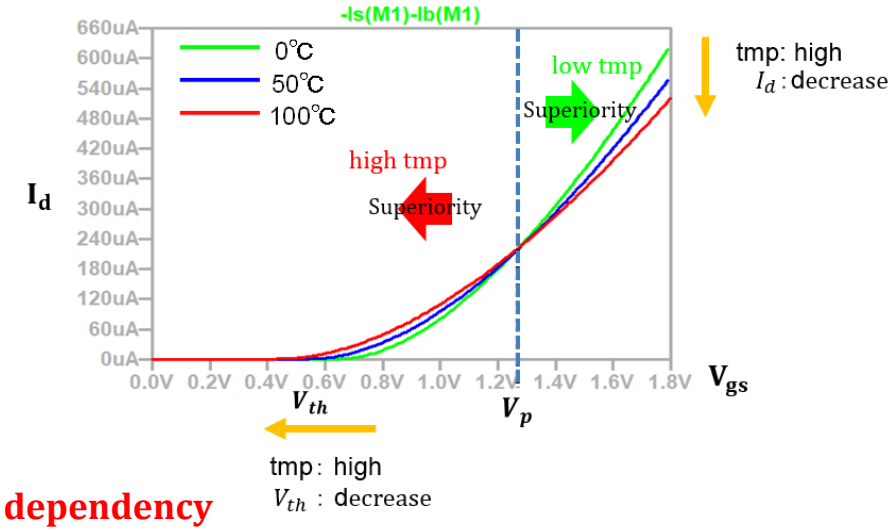
Auto Bias setting
5minute
（60s/1Tr searching for 10 L cases）

Bias Adjustment
0 ～ 1minute
（60s/1Tr searching）

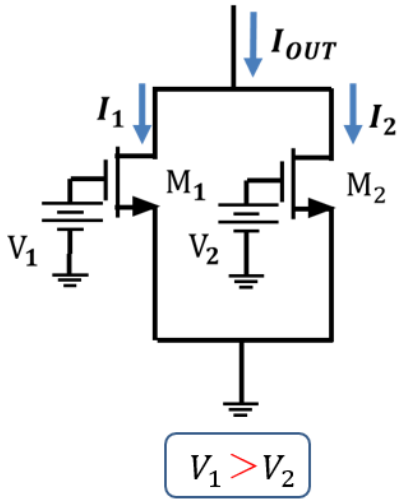
2 Experiments in TPSco 65nm PDK

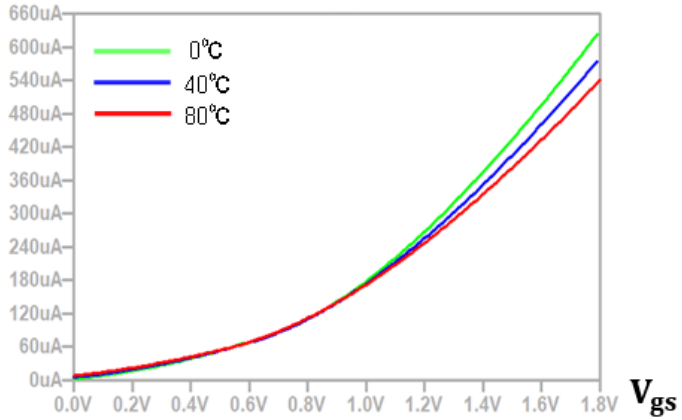
2. MOS reference current sources that are insensitive to temperature variation





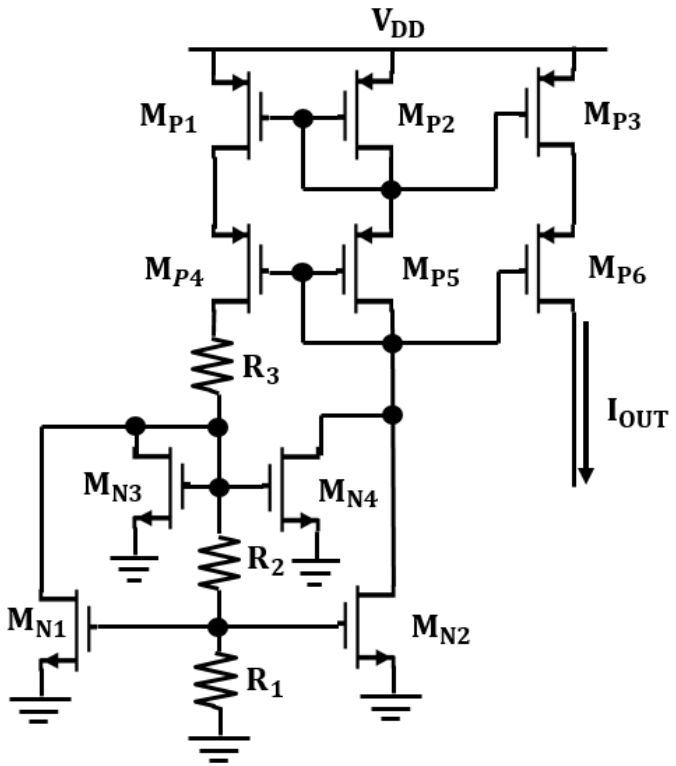
Cancel the temperature dependency





Iout（output Current）

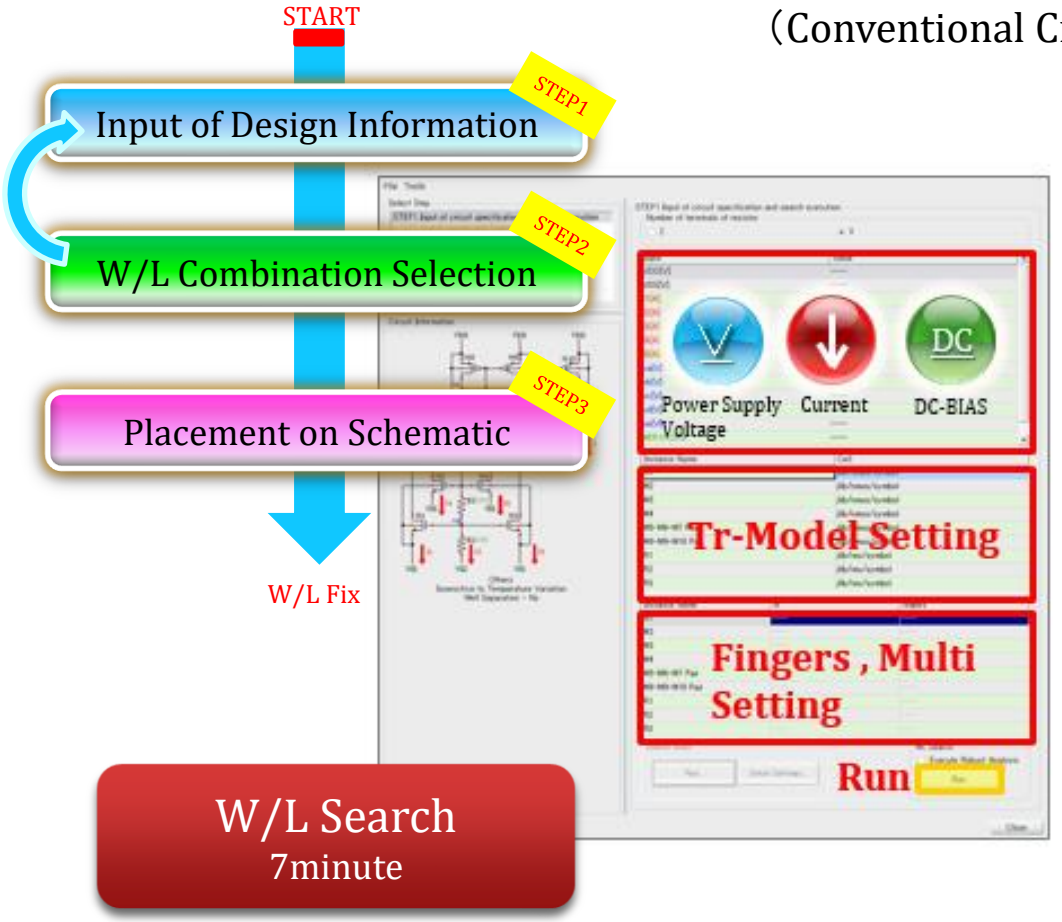
Circuit Registered to AnaCell



Trail performance by LW setting for researching

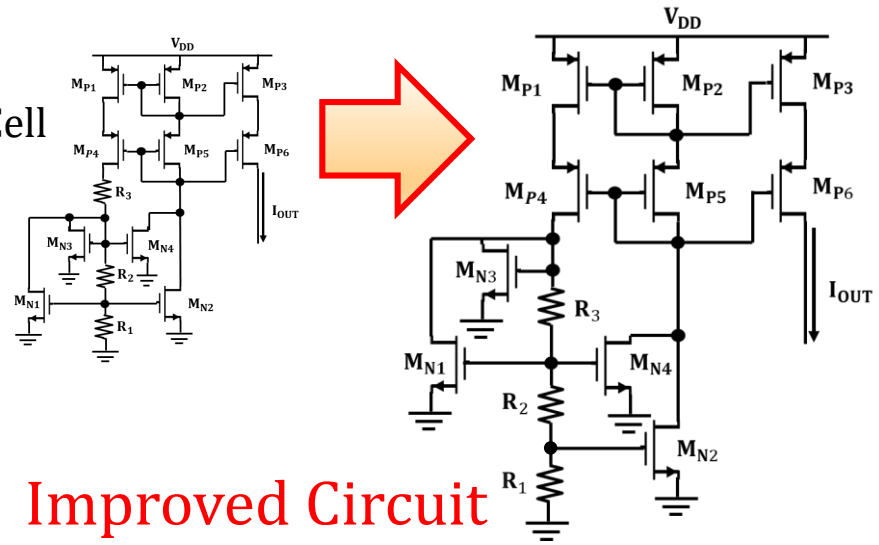
2 Experiments in TPSco 65nm PDK

AnaCell Design Flow

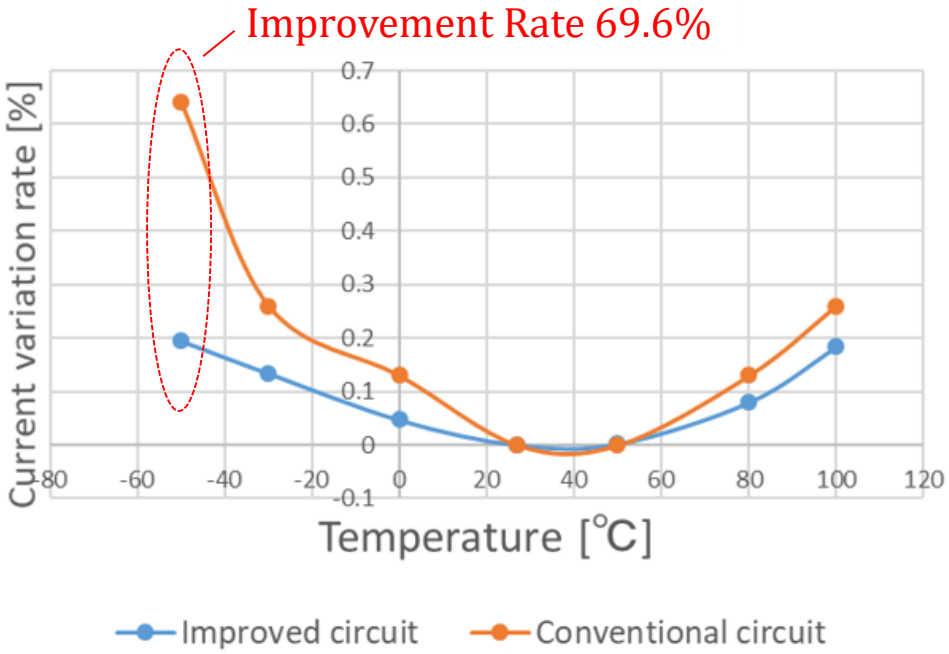


A diagram of the circuit actually converted to AnaCell

Circuit Registered to AnaCell
（Conventional Circuit）



Improved Circuit



Summary

- AnaCell can be applied for cell base analog design style but previously it requires designers some efforts and skill for DC bias setting.
- We propose auto DC bias setting which considers the freedom of design allowance (we call designability) with process free and designer only needs to set VDD and Current.
- This DC bias setting data would be reuse in other AnaCell's bias if condition is same, and it improves the design time significantly.
- This will promotes to auto analog generation without loss of multi performance and designer's intent.
- This design methodology changes the design style in proven circuits and also accelerates the research for new circuit.